Code No: 183AH **R22**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, February - 2024

COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to CSE, CE(SE), CSE(CS), CSE(DS), CSD)

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of **ten questions** (numbered from 2 to 11) **carrying 10 marks each**. From each unit, there are two questions and the student should answer one of them. Hence, the student should answer five questions from Part-B.

PART- A

(10 Marks)

1.a)	Which component is the brain of a computer?	[1]
b)	Define computer architecture.	[1]
c)	What is a microinstruction?	[1]
d)	List the three types of CPU organization.	[1]
e)	List out the types of Decimal Arithmetic Operations.	[1]
f)	Give example for floating point number.	[1]
g)	Which is the fastest memory in the memory hierarchy?	[1]
h)	What is an interrupt?	[1]
i)	What is omega network?	[1]
j)	List vector operations.	[1]

PART - B

(50 Marks)

2. How to construct a common bus system for four registers with multiplexers? Explain with necessary circuit diagram. [10]

OR

3.a) Explain about the shift micro operations.
b) Describe the phases in instruction cycle. [5+5]

4. Describe the general configuration of a microprogrammed control unit with the help of a block diagram. [10]

OR

5. Explain about the different types of addressing modes. [10]

6. Demonstrate addition and subtraction operations on sign magnitude data. [10]

OR

7. Explain the floating point operations with examples. [10]

8. Make a comparison of strobe control and handshaking methods. [10]

OR

9. Explain the utility of direct memory access controller with necessary diagram. [10]

10. Demonstrate various hazards of instruction pipeline and suggest mechanisms to avoid them. [10]

OR

11. Make a comparison of cross bar switch and hyper cube interconnection for a multiprocessor system. [10]

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